

REMARKS

Claims remaining in the present patent application are Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59. Claims 1, 3 and 11 are amended. Applicants note that no new matter is added as a result of the amendments presented herein. Applicants respectfully request reconsideration of the present application in view of the amendments presented herein and the following remarks.

Claim Objections

Claims 1 and 11 are objected to because of the phrase “plurality of functionalities.” Applicants respectfully submit that amendments presented herein correct these informalities, and respectfully solicit withdrawal of this objection.

35 USC § 112

1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 are rejected under 35 USC § 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. The rejection states that the “connection between the digital blocks themselves are not being clearly recited.”

Applicants respectfully traverse. Applicants respectfully assert that Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 recite that which is novel as well as

those necessary structural cooperative relationships of elements necessary to practice the invention, as required by 35 USC § 112. For example, it is well understood to couple a plurality of functional units to a bus.

Applicants respectfully assert that Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59 comply with 35 USC § 112, and respectfully solicit withdrawal of this rejection.

DOUBLE PATENTING REJECTION

Claims 42 and 35 are rejected under the judicially created (non-statutory) doctrine of obviousness-type double patenting as being unpatentable over Claims 1 and 8, respectively, of U.S. Patent No. 6,742,220 (CYPR-CD00169). A terminal disclaimer in compliance with 37 CFR §1.321 is being submitted concurrent with the instant response, thereby obviating the double patenting rejection.

35 U.S.C. § 103

Claims 1, 37 and 52 stand rejected under 35 USC § 103(a) as being allegedly unpatentable over Tzori (US 5,748,875, "Tzori") in view of Insenser Farre et al. (US 5,748,875, "Insenser"). Applicants have reviewed the cited references and respectfully assert that embodiments in accordance with the present invention as recited in Claims 1, 37 and 52 are patentable over Tzori in view of Insenser.

Applicants respectfully assert that Tzori and Insenser are non-analogous art, and that therefore the proposed combination of Tzori in view of Insenser is improper. Insenser is directed to “a user programmable integrated circuit” (Abstract). In contrast, Tzori is directed to a “digital logic simulation/emulation system.” Applicants respectfully assert that one of ordinary skill in the art would not seek to improve Tzori’s “digital logic simulation/emulation system” from the field of “user programmable integrated circuits,” as taught by Insenser.

As Tzori and Insenser are non-analogous art, Applicants respectfully assert that the proposed combination of Tzori in view of Insenser is improper, and that all rejections dependent upon Tzori in view of Insenser are therefore overcome. For this reason, Applicants respectfully assert that Claims 1, 37 and 52 overcome the rejections of record, and respectfully solicit allowance of these Claims.

In addition, Applicants respectfully assert that Tzori is non-analogous art per *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992). Per *In re Clay*, a reference must “(commend) itself to an inventor’s attention in considering his problem.” Applicants respectfully assert that Tzori is directed to a “digital logic simulation/emulation system.” (Abstract). Applicants do not find the systems of simulation taught by Tzori to commend Tzori to Applicants in consideration of Applicants’ problem.

Applicants respectfully assert that Tzori would not commend itself to one of ordinary skill in the art in consideration of the problems solved by the present invention, due to the myriad well known differences between systems for simulating hardware and actual hardware, as disclosed and claimed in the present application.

Applicants respectfully assert that the citation of Tzori is improper, and that all rejections dependent upon Tzori are therefore overcome. For this reason, Applicants respectfully assert that Claims 1, 37 and 52 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that there is no motivation to combine Tzori in view of Insenser, as proposed by the rejection. The rejection proposes the modification to “includ(e) the analog blocks as claimed.” The language of the rejection indicates that the claims of the present application improperly guided the construction of the rejection.

Moreover, Tzori is directed to a system for simulation/emulation of digital logic (Title, Abstract, *inter alia*, emphasis added). Applicants respectfully assert that one of ordinary skill in the art would not be motivated to improve simulation/emulation of digital logic by the addition of analog function blocks, as proposed by the rejection.

Per *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ2d 1438, 1442 (Fed. Cir. 1991), “[A] proper analysis under § 103 requires, *inter alia*, consideration of... whether the prior art would have suggested to those of ordinary skill in the art that they should make the claimed composition or device, or carry out the claimed process.” Regardless of the type of disclosure, the prior art must provide some motivation or suggestion to one of ordinary skill in the art to make the claimed invention in order to support a conclusion of obviousness.

As there is no suggestion in the art to make the proposed modification, Applicants respectfully assert that the rejection implies impermissible hindsight to forge a combination of references guided only by the disclosure and claims of the present application.

With respect to Claim 1, Applicants respectfully assert that the rejection improperly equates Tzori’s “Pod 32” with the recited “bus.” Importantly, “pod 32” is not described by Tzori as a “bus.” As taught by Tzori:

hardware pod 32... is adapted to receive a digital logic IC by a zero insertion force (“ZIF”) IC socket 34. In addition to the IC socket 34, the hardware pod 32 illustrated in FIG. 1 includes two (2) configurable-logic ICs 36a and 36b.

The hardware pod 32 further includes a central processing unit (“CPU”) 44 that preferably includes an Integrated Device Technology, Inc., of Santa Clara, Calif. R3081 MIPS R3000 derivative RISC microprocessor together

with other ancillary ICs. A microprocessor bus 46 couples the CPU 44 to a read only memory ("ROM") 48, a random access memory ("RAM") 52 and to a communication port 54, which is preferably an Sonic Ethernet IC marketed by National Semiconductor, Inc. of Santa Clara, Calif. The ROM 48, which provides 512K bytes of storage, holds only a minimum computer program required to boot the CPU 44 sufficiently to permit receiving additional computer programs through the communication port 54. (column 8, lines 25-47)

As understood by Applicants, "pod 32" is a printed circuit board comprising at least six integrated circuits and other components; including a socket for another IC, as described above and in Figure 1. Applicants respectfully assert that one of ordinary skill in the art would not understand "pod 32" as the recited "bus."

As is known by those of ordinary skill in the art, the recited "bus" does not consist of an "IC socket," "two (2) configurable-logic ICs," "CPU 44," "ROM 48," RAM 52" and "Ethernet IC 54." While Tzori may teach a generic "bus," Tzori teaches that "Pod 32" is not a bus. Consequently, the couplings to the recited "bus," set forth by the limitations of Claim 1, are not and cannot be taught or fairly suggested by "pod 32" as alleged by the rejection.

Applicants respectfully assert that Insenser fails to remedy this deficiency of Tzori, and note that the rejection does not allege such remedy.

For this additional reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 1, Applicants respectfully assert that Tzori actually teaches away from embodiments of the present claimed invention, as recited by Claim 1. As understood by Applicants, Tzori uses at least two bus structures to couple the various elements. For example, “microprocessor bus 46 couples the CPU 44 to a read only memory (‘ROM’) 48, a random access memory (‘RAM’) 52 and to a communication port 54,” while “stimulus/response data-bus 278” couples the CPU 44 to other elements of pod 32. In teaching the use of at least two busses to couple to such varied elements, Tzori actually teaches away from embodiments of the present claimed invention that recite coupling a microprocessor, a memory and a plurality of functional units to a single bus, as recited by Claim 1.

For this further reason, applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further still with respect to Claim 1, Applicants respectfully assert that Tzori actually teaches away from embodiments of the present claimed invention, as recited by Claim 1. Claim 1 recites “a microcontroller circuit.” As known by those of ordinary skill in the art, a microcontroller is a single IC. In contrast, Tzori teaches functions such as a CPU, ROM, RAM, communications and configurable logic in separate integrated circuits.

In teaching the use of multiple integrated circuits, Tzori actually teaches away from embodiments of the present claimed invention that recite a single integrated circuit, as recited by Claim 1. Moreover, Tzori teaches an “IC socket 34” as a part of “pod 32.” As is known by those of ordinary skill in the art, such a socket cannot be integrated into the recited “microcontroller.” In this additional manner, Tzori again teaches away from embodiments of the present claimed invention that recite a single integrated circuit, as recited by Claim 1.

For these further still reasons, applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further yet still with respect to Claim 1, Applicants respectfully assert that Tzori in view of Insenser fails to teach or fairly suggest the claimed limitation “an interconnect wherein said interconnect is dynamically configurable and programmable” as recited by Claim 1. The rejection alleges that Tzori “trace 42” and “data-bus 278” fairly suggest this instant limitation. Applicants respectfully traverse. Applicants find no teaching in Tzori that either “trace 42” or “data-bus 278” is “dynamically configurable and programmable” as recited by Claim 1. Applicants respectfully note that the rejection fails to provide a citation for such alleged teaching. As understood by Applicants, “trace 42” and “data-bus 278” are merely wiring traces on a printed circuit board. As is well known to those of

ordinary skill in the art, printed circuit board traces lack dynamic configuration and programmability.

Applicants respectfully assert that Insenser fails to remedy this deficiency of Tzori, and note that the rejection does not allege such remedy.

For this further yet still reason, applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Still further with respect to Claim 1, Applicants respectfully assert that Tzori in view of Insenser fails to teach or fairly suggest the claimed limitation “configured with a single register write operation” as recited by Claim 1. While Tzori may teach “load(ing)... configuration data...into the configurable-logic ICs 36a and 36b,” Tzori is completely silent as to the number of register write operations required to perform this task. More specifically, Tzori does not teach configuration “with a single register write operation” as recited by Claim 1.

Applicants respectfully assert that Insenser fails to remedy this deficiency of Tzori, and note that the rejection does not allege such remedy. In fact, with respect to another rejection, in section 18, the rejection concedes, “Insensers [sic] did not specifically showed [sic] single write operation as claimed.”

For this still further reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

While not rejected under the present grounds of rejection, Applicants respectfully assert that Claims 2 – 10 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claim 37 overcomes the rejections of record for at least the rationale previously presented with respect to Claim 1, and respectfully solicit allowance of this Claim.

While not rejected under the present grounds of rejection, Applicants respectfully assert that Claims 38-41 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claim 52 overcomes the rejections of record for at least the rationale previously presented with respect to Claim 1, and respectfully solicit allowance of this Claim.

While not rejected under the present grounds of rejection, Applicants respectfully assert that Claim 57 overcomes the rejections of record by virtue of its dependency, and respectfully solicit allowance of this Claim.

In addition with respect to Claim 52, Applicants respectfully assert that Tzori in view of Insenser fails to teach or fairly suggest the claimed limitation “a microcontroller comprising a non-volatile memory,” as recited by Claim 52. As previously presented with respect to Claim 1, Tzori does not teach a microcontroller. In contrast, Tzori teaches a system comprising multiple separate integrated circuits.

For this additional reason, Applicants respectfully assert that Claim 52 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Insenser Farre et al., (U.S. Patent No. 6,460,172 “Insenser”) in view of Furtek et al., (U.S. Patent No. 5,894,565 “Furtek”) and further yet in view of van der Wal et al., (U.S. Patent No. 6,188,381 “van der Wal”). Applicants have reviewed the cited references and respectfully assert that embodiments in accordance with the present invention as recited in Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 are patentable over Insenser in view of Furtek and further still in view of van der Wal.

Applicants respectfully assert that van der Wal is non-analogous art per *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992). Per *In re Clay*, a reference must “(commend) itself to an inventor’s attention in considering his problem.” Applicants respectfully assert that van der Wal is directed to a “real time

modular video processing system.” (Abstract). Applicants do not find the video processing systems taught by van der Wal to commend van der Wal to Applicants in consideration of Applicants’ problem. For example, the claims of the present invention are not directed to video processing.

Applicants respectfully assert that van der Wal would not commend itself to one of ordinary skill in the art in consideration of the problems solved by the present invention, due to the myriad well known differences between video processing systems and configurable microcontrollers, as disclosed and claimed in the present application.

Applicants respectfully assert that the citation of van der Wal is improper, and that all rejections dependent upon van der Wal are therefore overcome. For this reason, Applicants respectfully assert that Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 overcome the rejections of record, and respectfully solicit allowance of these Claims.

With respect to Claim 1, Applicants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or fairly suggest the claimed limitation of a bus coupling a non-volatile memory and a plurality of functional units, as recited by Claim 1. The rejection alleges that Insenser’s “optimized interface 9” is such a bus. Applicants respectfully traverse.

Insenser teaches, “optimized interface 9 (connects) the microprocessor core to the programmable cells and other on-chip peripherals 10” (column 2 lines 14-25). Importantly, “optimized interface 9” is not taught to couple the memory. Consequently, in consideration of all the limitations of bus coupling recited in Claim 1, “optimized interface 9” is not the recited “bus.” Moreover, no teaching of Insenser meets the claimed limitations of a “bus” as recited by Claim 1.

Applicants respectfully assert that neither Furtek nor van der Wal remedies this deficiency of Insenser, and note that the rejection does not allege such remedy.

For this additional reason, applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Further with respect to Claim 1, Applicants respectfully assert that Insenser in view of Furtek and further still in view of van der Wal fails to teach or fairly suggest the claimed limitation of a non-volatile memory coupled to a bus, as recited by Claim 1. The rejection concedes that Insenser “did not specifically showed [sic] the non-volatile memory as claimed.”

To correct this deficiency of Insenser, the rejection proposes to use the non-volatile memory 83 of Furtek. However, “dedicated function element 83” is placed “at the corners of each block 15 of logic cells 11 in the space provided at the intersections of rows and columns of repeaters 27 bounding the blocks 15” (column

11, lines 57-67). However, Insenser teaches a “RAM memory 1 for data and programs.” Applicants respectfully assert that the non-volatile memory taught by Insenser is ill-suited in both construction and logical placement for the function required by Insenser. Consequently, the proposed replacement would render the primary reference incapable of performing its intended function.

Per *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959), “if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious.”

As the proposed modification of Insenser in view of Furtek fails to establish *prima facie* obviousness, Applicants respectfully assert that all rejections dependent upon van Insenser in view of Furtek are therefore overcome. For this reason, Applicants respectfully assert that Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Still further with respect to Claim 1, Applicants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or fairly suggest the claimed limitation of a “a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being

configured with a single register write operation,” as recited by Claim 1. The rejection concedes that “Insensers [sic] did not specifically showed [sic] single write operation as claimed.”

To correct this deficiency of Insenser, the rejection proposes to use a write operation taught by van der Wal.

The cited passage (Col. 10, lines 30-38) of van der Wal recites:

These 10 bits represent the 8 bits of data and 2 bits of HA and VA timing in the format described above. In a preferred embodiment, the crosspoint switch 202 is implemented using 10 I-CUBE IQ96 crosspoint switch devices. Each of these devices provides a reconfigurable crosspoint switch for a single bit of the 10 bits of video data. These devices are configured so one control register write is capable of switching all 10 bits of data in all 10 IQ96 devices simultaneously. (emphasis added)

Applicants respectfully assert that the rejection misinterprets this disclosure as teaching the configuration or reconfiguration of a device with a single register write, as in Independent Claim 1. In contrast, this cited passage is directed to one control register write that is capable of switching all bits of video data in all devices simultaneously.

According to the passage, 10 (ten) I-CUBE IQ96 crosspoint switch devices implement the crosspoint switch 202. Moreover, each I-CUBE IQ96 crosspoint switch device provides a reconfigurable crosspoint switch for a single bit of the 10 bits of video data. Further, the 10 (ten) I-CUBE IQ96 crosspoint switch devices are configured as a whole in a manner described by the phrase which begins after the word “so” in the last sentence of the passage. That is, the phrase, “one control register write is capable of switching all 10 bits of [video] data in all 10 IQ96 devices simultaneously” (emphasis added), refers to the operation of the 10 (ten) I-CUBE IQ96 crosspoint switch devices as a whole.

Thus, there is no support for the rejection’s assertion that the passage teaches, “single control register write for reconfiguring all functional blocks or devices.” The one control register write in the passage is described as being capable of switching all 10 bits of video data in all 10 IQ96 devices simultaneously instead of reconfiguring functional blocks or devices. While the passage notes that bits of video data are switched simultaneously with the one control register write, the passage fails to describe any relationship between the one control register write and configuration (or reconfiguration) of the individual I-CUBE IQ96 crosspoint switch device. Use of the term “switching” corresponds to each I-CUBE IQ96 crosspoint switch device having an “on state” and an “off state.”

Therefore, each I-CUBE IQ96 crosspoint switch device must be configured/reconfigured with respect to its input and output ports via its

corresponding control register in some manner that is neither described nor expressly/implicitly referred as being a single control register write. Thus, van der Wal does not teach or fairly suggest that a digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation, as in the invention of Independent Claim 1.

For this still further reason, Applicants respectfully assert that Claim 1 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claims 2 – 10 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 4 and 7, Applicants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or fairly suggest the claimed limitation of “user input” as recited by Claims 4 and 7. The cited references are silent as to user interaction.

For this additional reason, Applicants respectfully assert that Claims 4 and 7 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Independent Claims 11, 17, 35, 37, 42, 51, and 52 overcome the rejections of record for at least the rationales previously presented with respect to Claim 1. More particularly, Independent Claims 11, 17, 35, 37, 42, 51, and 52, are directed to digital logic whose digital function is “configured with a single register write operation.” Applicants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or fairly suggest this instant limitation.

Accordingly, Applicants respectfully assert that Claims 11, 17, 35, 37, 42, 51, and 52 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Applicants respectfully assert that Claims 13-16, 18, 20-21, 23-34, 36, 38-41, 43-49, and 57 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 13-16, Applicants respectfully assert that Insenser in view of Furtek and further yet in view of van der Wal fails to teach or fairly suggest the claimed limitation of “user input” as recited by Claims 13-16. The cited references are silent as to user interaction.

For this additional reason, Applicants respectfully assert that Claims 13-16 overcome the rejections of record, and respectfully solicit allowance of these Claims.

In addition with respect to Claims 20 and 36, the rejection improperly equates “probing” as taught by Insenser with the recited coupling of programmable digital circuit blocks and programmable analog circuit blocks. In fact, the rejection incorrectly characterizes Insenser’s teaching. The rejection alleges Insenser to teach, “digital circuit blocks could probed with the analog circuit.” In contrast, Insenser actually teaches, “[a]ny point inside the digital blocks or the analog subsystems can be proged (by the microprocessor).” (column 3 lines 41-44). Applicants respectfully assert that “probing” by a microprocessor does not teach or fairly suggest coupling programmable digital circuit blocks to programmable analog circuit blocks, as recited by 20 and 36.

For this additional reason, Applicants respectfully assert that 20 and 36 overcome the rejections of record, and respectfully solicit allowance of these Claims.

Claims 58-59 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Insenser Farre et al., (U.S. Patent No. 6,460,172 “Insenser”) in view of Gamal et al., (U.S. Patent No. 5,754,826 “Gamal”) and further in view of van der Wal et al., (U.S. Patent No. 6,188,381 “van der Wal”). Applicants have reviewed the cited references and respectfully assert that embodiments in accordance with the present invention as recited in Claims 58-59 are patentable over Insenser in view of Gamal and further in view of van der Wal.

Applicants respectfully reiterate that the citation of van der Wal is improper as previously presented, and that all rejections dependent upon van der Wal are therefore overcome. For this reason, Applicants respectfully assert that Claims 58-59 overcome the rejections of record, and respectfully solicit allowance of these Claims.

With respect to Claim 58, Applicants respectfully assert that Insenser in view of Gamal and further in view of van der Wal fails to teach or fairly suggest the claimed limitation of a "a dynamically configurable and programmable digital functional block coupled to said interconnect, wherein said dynamically configurable and programmable digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation," as recited by Claim 1. The rejection concedes that "neither Insensers [sic] nor Gammal [sic] showed single write operation as claimed."

To correct this deficiency of Insenser and Gamal, the rejection proposes to use a write operation taught by van der Wal.

The cited passage (Col. 10, lines 30-38) of van der Wal recites:

These 10 bits represent the 8 bits of data and 2 bits of HA and VA timing in the format described above. In a preferred embodiment, the crosspoint switch 202 is implemented using 10 I-CUBE IQ96 crosspoint switch devices. Each of

these devices provides a reconfigurable crosspoint switch for a single bit of the 10 bits of video data. These devices are configured so one control register write is capable of switching all 10 bits of data in all 10 IQ96 devices simultaneously. (emphasis added)

Applicants respectfully assert that the rejection misinterprets this disclosure as teaching the configuration or reconfiguration of a device with a single register write, as in Independent Claim 1. In contrast, this cited passage is directed to one control register write that is capable of switching all bits of video data in all devices simultaneously.

According to the passage, 10 (ten) I-CUBE IQ96 crosspoint switch devices implement the crosspoint switch 202. Moreover, each I-CUBE IQ96 crosspoint switch device provides a reconfigurable crosspoint switch for a single bit of the 10 bits of video data. Further, the 10 (ten) I-CUBE IQ96 crosspoint switch devices are configured as a whole in a manner described by the phrase which begins after the word “so” in the last sentence of the passage. That is, the phrase, “one control register write is capable of switching all 10 bits of [video] data in all 10 IQ96 devices simultaneously” (emphasis added), refers to the operation of the 10 (ten) I-CUBE IQ96 crosspoint switch devices as a whole.

Thus, there is no support for the rejection’s assertion that the passage teaches, “single control register write for reconfiguring all functional blocks or devices”. The one control register write in the passage is described as being capable

of switching all 10 bits of video data in all 10 IQ96 devices simultaneously instead of reconfiguring functional blocks or devices. While the passage notes that bits of video data are switched simultaneously with the one control register write, the passage fails to describe any relationship between the one control register write and configuration (or reconfiguration) of the individual I-CUBE IQ96 crosspoint switch device. Use of the term “switching” corresponds to each I-CUBE IQ96 crosspoint switch device having an “on state” and an “off state”.

Therefore, each I-CUBE IQ96 crosspoint switch device must be configured/reconfigured with respect to its input and output ports via its corresponding control register in some manner that is neither described nor expressly/implicitly referred as being a single control register write. Thus, van der Wal does not teach or fairly suggest that a digital functional block is configurable to perform any one of a plurality of predetermined digital functions upon being configured with a single register write operation, as in the invention of Independent Claim 1.

For this still further reason, Applicants respectfully assert that Claim 58 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

Applicants respectfully assert that Claim 59 overcome the rejections of record by virtue of their dependency, and respectfully solicit allowance of these Claims.

In addition with respect to Claim 59, Applicants respectfully assert that fails to teach or fairly suggest the claimed limitation of a “time base” as recited by Claim 59. The rejection improperly equates “operating frequency of filters” as taught by Insenser with the recited “time base.”

Applicants respectfully assert that the taught “operating frequency of filters” is unrelated to the recited “time base,” as understood by those of ordinary skill in the art. For this additional reason, Applicants respectfully assert that Claim 59 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

CONCLUSION

Claims remaining in the present patent application are Claims 1-11, 13-18, 20-21, 23-49, 51-52, and 57-59. Applicants respectfully request reconsideration of the above captioned patent application in view of the amendments and remarks presented herein.

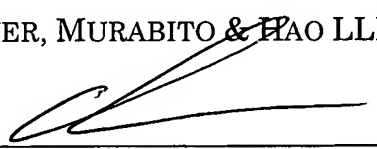
The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

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Respectfully submitted,

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